29.3 Increasing Microprocessor Speed by Massive Application of On-Die High-K MIM Decoupling Capacitors

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The need for improved on-die power supply integrity increases with technology advances due to large demand on the power supply network to provide instantaneously large currents. The problem is one of L*di/dt voltage droops induced by the effective inductance of the package power pins. Packaging technology can only provide partial relief to solve the inherent problem of instantaneous delivery of current. Active circuitry can alleviate the problem at a high circuit design and development cost [1]. This problem is further exacerbated in SOI for small, fast die due to the inherent junction capacitance and well capacitance loss relative to bulk Si. In this paper, we propose and present results of the implementation of massively pervasive On-Die metal-highK insulator-metal decoupling capacitor (high-K MIM decap) for improved maximum processor Core frequency.

The paper will present the simulations, physical implementation, technology information, and processor Fmax results that show an increase of ~10% Fmax induced by inclusion of the high-K MIM decap. Simulation results for application to PLL and I/O circuits and expected benefits are also addressed.

The electrical macro network used for assessing the on-die power droop of a microprocessor is presented in Fig. 29.3.1 [2]. It consists of a lumped electrical model of the package RLC network, lumped RC representation for any on-die decap, resistive on-die power distribution resistance and a switching current source representation of the logic gates. The processor analyzed only has 40nF of on-die decap due to the small area. The predicted on-die voltage droop associated with a 1.5V 25W 130nm SOI microprocessor is in the order of 19% to 21% depending on chip leakage (Fig. 29.3.2). To approach a 5% Vdd droop limit requires an on-die decap larger than 2μF. Notice that the processor leakage, whether logic gate or decap dominated, can have close to a 3% impact on the internal supply AC collapse.

The MIM capacitor used to decouple the internal power supply is shown in Fig. 29.3.3. The 8fF/μm^2 planar MIM capacitors of the 90nm SOI technology are formed by physical vapor deposition of alternating layers of HfO_2 and Ta_2O_5 dielectrics between TaN electrodes [3]. The performance of the MIM decap is dictated by the frequency response, which is dictated by the contact spacing. Given a target cutoff frequency, the contact spacing can be chosen to the desired frequency response. Yield and static leakage (I_{DD}) performance of microprocessors that include core logic MIM are equivalent to non-MIM parts, while performance degrades if SiO_2 thickness of the gate-oxide decoupling capacitors is reduced.

A 90nm SOI microprocessor only contained 25nF of on-die SiO_2-based decap. The addition of the MIM decap increased the Core Vdd decap by 250nF. DC leakage of the MIM capacitors is 2.5 to 3 orders of magnitude lower than gate-oxide caps, leading to lower Core Vdd leakage at enhanced frequency response. MIM capacitor integration was 'non-invasive' with respect to the existing design features. The processor mask set was altered by addition of the MIM module between the metallization layer below last metal and the second last metal. As such, the MIM plates are porous with via holes as needed to maintain the original mask set signal routing between the last two metals. Various MIM plates were created for different voltage islands within the processor. (Fig. 29.3.4).

Addition of MIM decap inherently changes the supply network noise voltage signature effectively shifting the timing paths. In Fig. 29.3.5, it is shown that a large Core Vdd voltage droop is dampened from 250mV to 156mV with the addition of MIM decap. This measurement is done by probing exposed C4 Core Vdd from the microprocessor while executing the same tests, effectively bypassing the package. Measured microprocessor $F_{max,}$ increases up to approximately 8%, and in proportion to the amount of core decap, are achieved (Fig. 29.3.6). These increases are equivalent to a transistor node improvement in performance.

Application of MIM decap to the I/O supply should also provide improvement in I/O circuits and high speed interfaces. The simulated internal minimum voltage seen by a 90nm SOI 2.5V DDR I/O is plotted in Fig. 29.3.7. It shows that for a small amount of on-die I/O decap, a large internal di/dt voltage noise close to 50% of the I/O supply is present. It is also shown that use of package-mounted decap only improves the Vmin by 100mV. This DDR interface requires larger than 10nF of on-die decap to maintain the integrity of the supply network.

Other applications of MIM decap to PLL circuits help reduce PLL area, which is an issue for scaling of analog circuits, as capacitors with low leakage and low area are a must for integration into small die. For example, a 400pF filter capacitor occupies about 223×223μm^2 of area, as compared to a thick-oxide capacitor needed to limit gate capacitor leakage which occupies close to 223×760μm^2. This 3.4× area reduction is effectively a larger savings in die area since the MIM capacitor resides between the metal layers.

Inclusion of high-K MIM decap modules in 90nm SOI technology is shown to improve Fmax by close to 10%. Application of MIM decap to high speed I/O and PLL circuits can further enhance performance and area requirements in advanced technologies.

References:

[1] S. Naffziger, et al., "The Implementation of a 2-Core Multi-Threaded Itanium Family Processor," *ISSCC Dig. Tech. Papers*, pp 182-183, Feb., 2005.

[2] O. Mandhana, "Design Oriented Analysis of Package Power Distribution System Considering Target Impedance for High Performance Microprocessors," *EPEP Tech. Dig.*, pp. 273-276, 2001.

[3] D. Roberts, et al., "On-Chip MIM Decoupling Capacitor for High-Performance Power Distribution Grid," Proc. IEDM, accepted for presentation, 2005.

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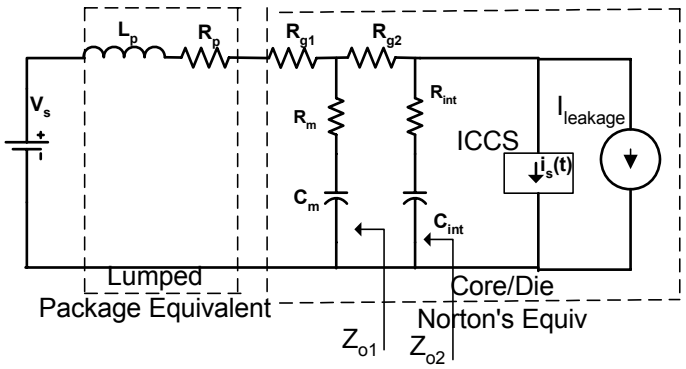

Figure 29.3.1: Processor package/die electrical macro model.

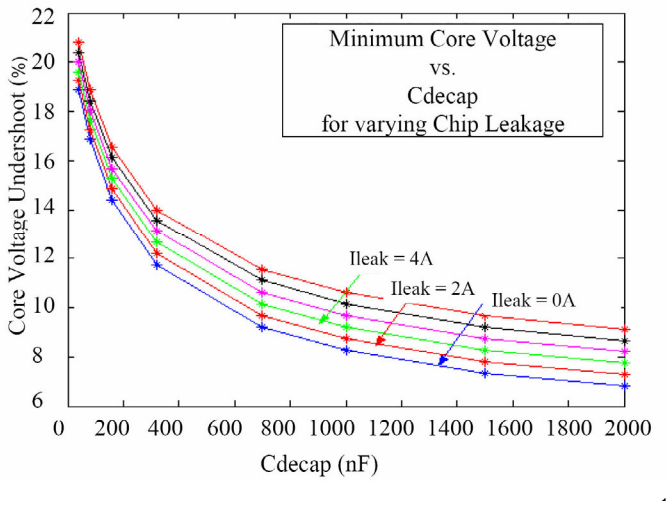

Figure 29.3.2: Simulated voltage reduction in internal processor voltage due to package di/dt noise as a function of Cdecap and Ileak.

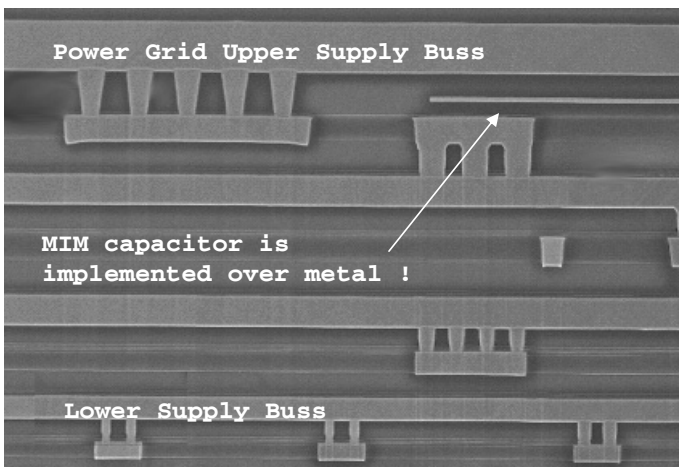

Figure 29.3.3: Die Cross-section of metallization stack for upper 8 metal levels showing integration of MIM into copper/low-K backend.

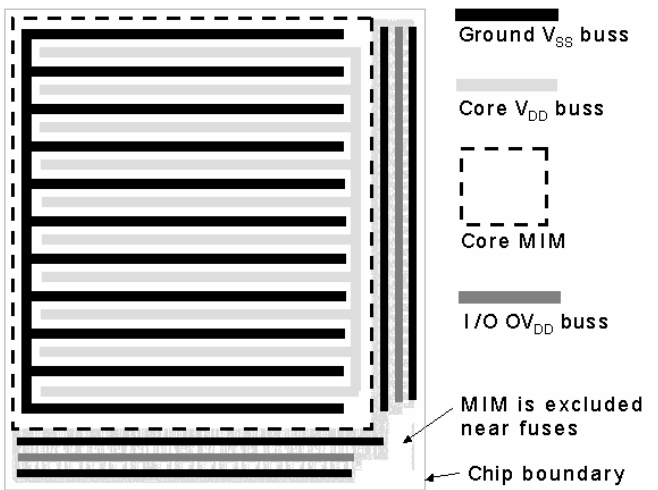

Figure 29.3.4: MIM decoupling capacitor voltage partitioning.

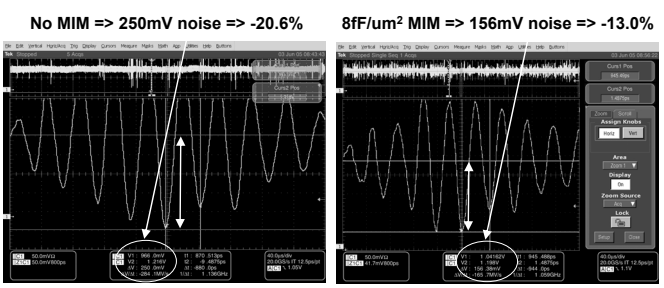

Figure 29.3.5: Measured core Vdd no MIM versus with MIM.

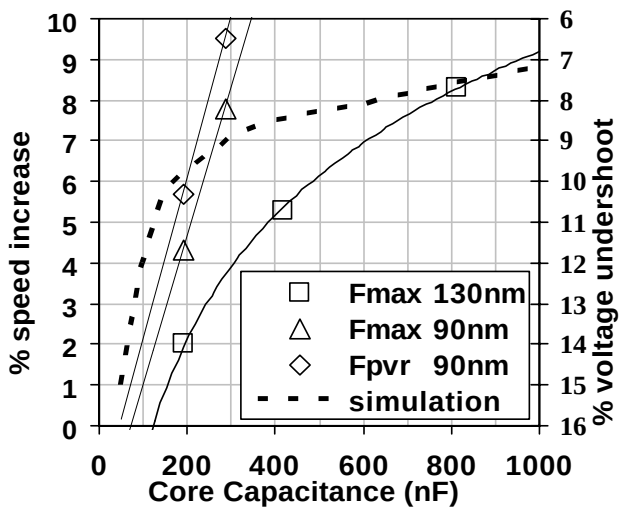

Figure 29.3.6: Fmax sensitivity to decap amount.

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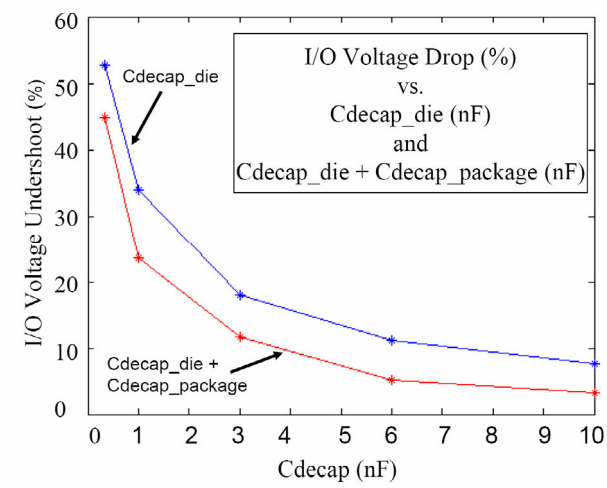

Figure 29.3.7: Simulated I/O Voltage reduction as function of internal decap and internal + package-mounted decap.

